

Abstract

A semiconductor device for performing an N-bit prefetch operation, N being a positive integer includes a data strobe buffering means for generating N number of align control signals based on a data strobe signal and a external clock signal; a receiving block in response to N-1 number of the align control signals for receiving N-bit data and outputting the N-bit data in a parallel fashion; and a outputting block 5 in response to the remaining align control signal for receiving the N-bit data in the parallel fashion and synchronizing the N-bit data with the remaining align control signal having a $N/2$ external clock period to thereby generating the synchronized N-bit data as a prefetched data.

5